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# Apache Design and DA Integrated Seminar

**Date:** Wednesday, February 20, 2013 - 9:00am - 12:00pm EST
**Location:** Ottawa, Canada

**Manage Power, Noise and Reliability for Advanced Microelectronic Subsystems**

Power efficiency and power integrity are key aspects of today's microelectronics design methodology. Accurately predicting power consumption from an early design stage and simulating the impact of power/ground noise on the performance of an IC is critical to the success of advanced microelectronic designs. Integration of analog and mixed signal modules such as radios, USBs and high-speed I/Os along with digital IC subsystems is also challenging given the sensitive nature of the analog modules. Shared power delivery networks and substrates between analog and digital modules in an IC pose a high risk for noise corruption. Simulating the entire IC subsystem with the digital and analog components ensures the fidelity of the power delivery and substrate network.

IC-aware system design and system-aware IC design is a major paradigm shift from existing design methodologies. With 3D-ICs and multi-chip package modules going mainstream, it is increasingly important to simulate the complete impact of Chip, Package and System for power and signal integrity. Ensuring reliability of ICs is another critical requirement in the design methodology for both lifetime failures (Electromigration-EM) and event failures (Electrostatic Discharge-ESD). Reliability margins in sub-28nm technology nodes are rapidly decreasing for both EM and ESD, and simulation driven failure analysis is mandatory to ensure the proper operating lifetime and reliability of these ICs.

This seminar will explore the following aspects of power, noise and reliability from the IC to the System:

- A comprehensive RTL-to-Gate methodology for power optimization and closure of advanced microelectronic designs
- Advanced simulation techniques and tools for power noise validation using a Chip-Package-System approach
- Tools and methodologies for addressing IC reliability challenges such as EM, ESD and Electromagnetic Interference (EMI)

**Seminar Location:**

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