MEMS-enabled SoCs Drive Test Innovation

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The evolution of the micro-electro-mechanical systems (MEMS) industry is following a path similar to the maturation of the mixed-signal system-on-chip (SoC) industry. Demand for MEMS features, especially from the consumer market, is driving the integration of MEMS functionality into SoCs. The emergence of standard MEMS processes, the integration of MEMS design and verification functionality into mainstream electronic design automation (EDA) tools, and the availability of MEMS intellectual property (IP) will enable SoCs with multiple MEMS blocks or features.

The emergence of high-volume, low-cost SoC devices that include multiple MEMS transducers in the feature set present a difficult challenge for production test. Rather than integrating MEMS test capability into traditional SoC automatic test equipment (ATE), the diversity and complexity of physical stimuli required to test MEMS will result in a pipeline approach to test and a separation of electrical and MEMS testing. The need to simplify and reduce the cost of MEMS testing will drive innovation in MEMS design for test. The key trends driving current SoC testing will also be critical in the testing of integrated SoC/MEMS devices.

Historically, MEMS devices have been low-volume, high-complexity and high-value products that benefit from a line-based manufacturing approach. In a line-based manufacturing model, individual value-added manufacturing steps, including test, are collocated in a single manufacturing line. Traditional MEMS device manufacturing has product-specific test solutions collocated with assembly equipment. A key advantage of the line-based approach for early MEMS devices has been the early detection of process variation and precise functional testing. As MEMS processes mature and standard MEMS processes become available, this diminishes as a requirement.

As a product matures and transitions to high-volume, low-margin production, the line-based approach becomes prohibitive from a scalability and cost perspective. Scaling a line-based manufacturing model involves replicating the production line. With respect to test, this requires a duplication of dedicated custom test solutions. At this point, a cell-based manufacturing approach is advantageous from a cost, scalability and support perspective. For mainstream ICs, including SoC devices, cell-based manufacturing has long been the norm. Wafer fabs, assembly floors and production test houses make up a typical supply chain. Even within these major cells, the manufacturing flow involves sub-cells (e.g., photolithography, diffusion and etch).

The early stages of a cell-based manufacturing supply chain are under development in the MEMS industry as evidenced by the emergence of foundry access and MEMS packaging services. As the availability of standard MEMS processes and standard MEMS IP increases, the evolution of the MEMS industry into a cell-based manufacturing supply chain will accelerate. As with traditional ICs, assembly and production test will become separate services for MEMS devices.

The success of the manufacturing cell approach, with respect to test, lies with maximizing capital equipment utilization not only during production runs, but also over the entire amortization period of the equipment (and beyond). On a production test floor, this drives the industry to adopt general-purpose ATE. ATE has the benefit of being highly scalable and reconfigurable to manage demand fluctuations. In addition, the support costs of a common platform of ATE are much lower than a product-specific, custom test solution.

What Solution Will Emerge to Test SoCs with Integrated MEMS Features?

One approach originates from the integration industry sector that historically served the high-value, high-average selling price (ASP) MEMS sector by developing a fully customized test solution for every new MEMS device. This approach involves standardizing aspects of device handling (or probing) and electrical test and overlaying device-specific environmental interaction systems. This approach works well for basic MEMS devices where the electrical testing is relatively simple and the focus is on precision functional testing with environmental stimulus. However, this approach has numerous shortcomings when applied to a SoC device where electrical functionality is more complex. And when multiple MEMS features are included in a single SoC device, the approach breaks down altogether.

A second approach expands the capability of the current SoC ATE systems to include environmental stimulus and the measurement of MEMS transducers. This integrated SoC/MEMS tester approach also has numerous drawbacks. The complexity and settling time of environmental interactions creates lengthy test times and, consequently, high test costs. The use of parallelism (i.e., testing multiple devices at the same time) cannot fully alleviate this problem. Again, SoC devices with multiple transducers requiring diverse environmental stimuli are hardly conceivable.

Independent of the trend towards inclusion of MEMS-based functions, the existing paradigm for SoC testing is moving away from the traditional SoC ATE. The underlying challenges faced by SoC ATE vendors are complex. Larger SoC devices require more and more capability (i.e., higher capital) and longer test times (due to a higher element count). Adding this increased capability in an ATE system drives up both capital cost and test time, resulting in an exponential rise in test cost. Increasingly, successful device developers are treating production test as a design problem and eliminating the need for high-end SoC testers all together.

The solution for production testing of SoC devices with integrated MEMS features is not to adopt the current paradigm for SoC test, but rather adopt the emerging paradigm for SoC test. The emerging paradigm for SoC devices employs four basic principles that, in turn, enable simpler, lower cost ATEs:

- **Built-in self test (BIST)** has been employed for embedded memory BIST (mBIST) and digital logic (Scan) for many years. In general, BIST means including an on-chip circuit that verifies the correct structural fabrication of the device and provides a highly simplified electrical signature enabling a vastly simplified and, often, faster production

screen. Embracing the reality that the sole purpose of production test is to verify the absence of manufacturing defects is often the most difficult challenge for SoC developers.

- **Test access ports (TAPs)** can be created as a standalone input/output (I/O) or by muxing TAP functionality with system function-related I/O. Fundamentally, electrical access to BIST I/O or functional I/O of embedded blocks must be provided to enable practical production testing.

- **Built-out self test (BOST)** refers to the use of custom circuitry or instrumentation that is not fully integrated into either the SoC device or the ATE system. Usually, BOST is included on loadboards as custom circuitry or modules. Traditionally, BOST was frowned upon due to factory floor considerations such as scalability, calibration and maintenance. However, with SoC ATE instrumentation quickly losing ground to SoC device functionality, production test solutions, including BOST, are becoming common.

- **Pipelined test flows** directly address the mismatch of test instrument cost versus utilization by disassembling test into multiple stages. A major drawback of highly sophisticated SoC ATE systems is that the value and cost of any specific instrument is inversely proportional to its utilization and contribution to fault coverage. The principles of defect clustering dictate that the low-complexity tests such as supply current testing, direct current (DC) parametrics and low-speed signal tests capture the vast majority of the defect-related dropout and justifiably occupy the bulk of test time. The high-performance, high-cost instruments provide only incremental fault coverage along with a non-linear contribution to test cost while sitting idle for the majority of the test interval.

A pipelined approach disassembles testing into stages, each with a specialized environment and instrumentation. This enables the optimization of cost and utilization. The pipelined test approach is not a new concept, and many examples of pipelined test flows exist today. Probe, final test, multi-site test, ping-pong test and two-pass final test are all special cases of the pipelined test approach.

Pipelined test solutions for SoC/MEMS devices provide compelling cost and throughput numbers. Electrical test can be executed on traditional style ATE using new, low-cost ATE systems followed by environmental testing of transducer elements done as separate stages. Execution of the first purely electrical stage is done on traditional ATE, with the use of BIST, TAP and BOST, reducing the overall cost of test.

The maturation of BIST, TAP and BOST techniques enables the subsequent stages, where the environmental interaction is included for SoC transducer devices. By adopting the first three principles (BIST, TAP and BOST), a well-designed MEMS product benefits from simplification of the electrical interface during the environmental test, thus reducing the overall capital outlay of the environmental system to a negligible portion of the cost of test for these stages. With environmental stabilization time being a dominant cost factor, the use of mass parallelism during the environmental stage is paramount. Rather than using ATE, environmental test stages leverage TAP and BOST to configure devices and collect test data.

Taking into consideration the diversity of environmental stimuli required to test MEMS transducers, the use of a pipelined test flow becomes a requirement. A SoC with integrated MEMS transducers could require the exposure or measurement of any combination of pressure, temperature, motion, sound, light, fluids and radio frequency (RF). With the integration of multiple MEMS transducers on a single device, a single multi-purpose tester becomes a huge challenge.

The cost and complexity of applying environmental stimulus to test SoC/MEMS devices will drive innovation. More sophisticated BIST circuitry, in combination with empirical data, may support a reduced test suite. In the long term, advances in MEMS BIST could further reduce the environmental stages of the pipelined test flow solution. Ultimately, only characterization and on-going quality control would require environmental testing.

The evolution of SoC testing lies in the adoption of four basic principles: BIST, TAP, BOST and pipelined test. As traditional SoC testing moves in this direction, SoCs with MEMS elements benefit from this approach. Emerging high-volume, low-cost SoC devices with MEMS transducer elements can find a cell-based, mass-volume test solution.

About the Author

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